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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,671	08/07/2001	Shigeki Furuya	60188-084	1398

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EXAMINER
WARREN, MATTHEW E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/922,671	Applicant(s) FURUYA ET AL.	
	Examiner Matthew E. Warren	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cov r sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-37* is/are allowed.

6)☒ Claim(s) *22-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *01 July 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Amendment filed on July 1, 2002.

Drawings

The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on July 1 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 22-33 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not support the limitation that an "interconnect pattern is electrically isolated." In the

drawings (ex. Fig. 1C, interconnect 9) an interconnect looks to be electrically isolated, but is eventually connected to another interconnect (Fig. 1D, global interconnect 60). The specification (pg. 11, lines 11-21) states that the interconnects are connected to an upper interconnect layer for global routing, ultimately connecting basic cells together. If that alleged "electrically isolated" interconnect is connected to a global routing interconnect then it is not electrically connected further more. If that "electrically isolated" interconnect is not electrically connect to any component, then it is not an interconnect, it is just a metal layer. The term "interconnect" would then not properly identify the metal layer because in the art of semiconductors, interconnects are electrically connected between components.

Claims 25-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 25 contains the limitation that the "interconnect pattern is mutually connected electrically with an interconnect pattern of another CMOS cell." This limitation contradicts the limitation of the independent claim in which the interconnect is electrically isolated.

Claim 27 contains the limitation "wherein the interconnect pattern which intersects said higher interconnect pattern is electrically connected with a higher interconnect pattern except said higher interconnect patter which intersects said interconnect pattern." That phrase does not make sense because it seems to say that the interconnect pattern is connected with a higher interconnect pattern and then

another higher interconnect pattern and then it is not connected with the higher interconnect pattern.

Claims 26 and 27 also recite the limitation "The gate array semiconductor integrated circuit" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 22 and 23 as far as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Amishiro et al. (US 6,288,477 B1).

Amishiro et al. shows (figs. 5 and 6) a CMOS basic cell comprising an N-channel transistor region and a P-channel transistor region (5b and 5c) isolated from each other by an insulating film (2) on a substrate (1). An interconnect pattern (10d) exists between the two transistors and is formed in an uppermost interconnect layer (11). The

interconnect also extends along a direction horizontal to a boundary between the N-channel transistor region and the P-channel transistor region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24-33, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Amishiro et al. (US 6,288,477 B1) in view of the Applicant's Prior Art Figure 31 (APAF).

Amishiro et al. does not specifically disclose the power supply and master patterns of the device but is such items are necessary for the function of the semiconductor and well known in the art. However, the APAF 31 also shows a power supply (7), a master pattern , and another interconnect pattern different from the interconnect pattern. The another interconnect patter exists between the N-channel transistor and the master pattern and extends along a perpendicular direction relative to a boundary between two transistors. The another interconnect pattern is disconnected from the transistors and formed in an uppermost interconnect layer. The interconnect is also mutually connected with an interconnect pattern of another CMOS cell, the CMOS cell adjacent to the another CMOS cell. Two or more interconnect patterns are electrically connected by a higher interconnect pattern located in a layer higher than the

interconnect pattern. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the interconnect pattern of Amishiro by using power supply and alternate interconnect patterns as shown by the APAF to form connections to the various basic cells in the semiconductor device.

Amishiro et al. and the APAF show all of the elements of the claims except the method of fabricating the gate array. A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Allowable Subject Matter

Claims 34-37 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art references, alone or in combination, do not show a CMOS basic cell comprising a gate of one of N and P channel transistors having a hooked shape including a first bent part at one upper end portion and second bent part in an opposite side direction at a lower end and a diffusion region having a hooked shape having a first bent part at an upper portion and a second bent part in an opposite side direction at a lower portion wherein the upper portion of the gate is bent oppositely to the upper portion of the diffusion region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 22-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

MEW
October 7, 2002